

**Amendments To the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (canceled).  
Claim 2 (canceled).  
Claim 3 (canceled).  
Claim 4 (canceled).  
Claim 5 (canceled).  
Claim 6 (canceled).  
Claim 7 (canceled).  
Claim 8 (canceled).  
Claim 9 (canceled).  
Claim 10 (canceled).  
Claim 11 (canceled).  
Claim 12 (canceled).  
Claim 13 (canceled).  
Claim 14 (canceled).  
Claim 15 (canceled).  
Claim 16 (canceled).  
Claim 17 (canceled).  
Claim 18 (canceled).  
Claim 19 (canceled).  
Claim 20 (canceled).  
Claim 21 (canceled).  
Claim 22 (canceled).  
Claim 23 (canceled).  
Claim 24 (canceled).

Claim 25 (canceled).

Claim 26 (canceled).

1 Claim 27 (currently amended): A processing core of a processing system, employed in an  
2 audio and video encoder/decoder, for [processing information using] performing  
3 hardware-assisted context switching, comprising:

4 a processing unit;

5 an instruction cache for storing instructions for non-time-critical tasks and a  
6 code random access memory for storing instructions required for causing serving of time-  
7 critical tasks, the instruction cache and the code random access memory coupled to the  
8 processing unit;

9 a register group for updating status of registers related to time critical tasks;

10 and

11 another register group coupled to the processing unit,

12 wherein the processing unit need access status of registers only in the register  
13 group for execution of time-critical tasks thereby avoiding saving and restoring status of  
14 the another register group for execution of time-critical tasks.

1 Claim 28 (previously presented): The processing core according to Claim 27, wherein one  
2 of the time-critical tasks is providing additional data to a video engine unit during a video  
3 compression process.

1 Claim 29 (previously presented): The processing core according to Claim 28, wherein the  
2 additional data is provided to the video engine unit within a time interval of less than two  
3 microseconds.

1 Claim 30 (previously presented): The processing core according to Claim 27, wherein one  
2 of the non-time-critical tasks is multiplexing of audio and video streams.

1 Claim 31 (previously presented): The processing core according to Claim 27, wherein one  
2 of the one-time-critical tasks is demultiplexing Motion Picture Expert Group (MPEG)  
3 streams.

1 Claim 32 (previously presented): The processing core according to Claim 27, wherein the  
2 non-time-critical tasks are user interface application.

1 Claim 33 (previously presented): The processing core according to Claim 32, wherein one  
2 of the user interface applications is providing an on-screen display every two seconds.

1 Claim 34 (currently amended): A method of processing information [by a processing core  
2 for a processing system employed] using hardware-assisted context switching in an audio  
3 and video encoder/decoder, comprising:

4 providing a processing unit;

5 coupling an instruction cache and a code random access memory to the  
6 processing unit;

7 coupling a register group and another register group to the processing unit;

8 coupling a data memory and another data memory to the processing unit;

9 coupling a low priority interrupt controller and a high priority interrupt controller  
10 to the processing unit;

11 performing non-time-critical tasks through dedicated use by the processing unit of  
12 the instruction cache, the register group, the data memory, and the low priority interrupt  
13 controller;

14 performing time-critical tasks through dedicated use by the processing unit of the  
15 code random access memory, the another register group, the another data memory, and the  
16 high priority interrupt controller; and

17 accessing status of registers only in the register group for execution of time-critical  
18 tasks thereby avoiding saving and restoring status of the another registers for execution of  
19 time-critical tasks.

1 Claim 35 (previously presented): The method according to Claim 34, wherein performing  
2 time-critical tasks further comprises providing additional data to a video engine unit  
3 during a video compression process.

1 Claim 36 (previously presented): The method according to Claim 35, wherein providing  
2 additional data further comprises providing the additional data to the video engine unit  
3 within a time interval of less than two microseconds.

1 Claim 37 (previously presented): The method according to Claim 34, wherein performing  
2 non-time-critical tasks further comprises multiplexing of audio and video streams.

1 Claim 38 (previously presented): The method according to Claim 34, wherein performing  
2 non-time-critical tasks further comprises demultiplexing Motion Picture Expert Group  
3 (MPEG) streams.

1 Claim 39 (previously presented): The method according to Claim 34, wherein performing  
2 non-time-critical tasks further comprises performing user interface applications.

1 Claim 40 (previously presented): The method according to Claim 39, wherein performing  
2 user interface applications further comprises providing an on-screen display every two  
3 seconds.

1 Claim 41 (previously presented): An audio and video encoder/decoder, comprising:  
2 a processing system;  
3 a video engine unit and a video interface unit both coupled to the processing  
4 system;  
5 an audio engine unit and an audio interface unit both coupled to the processing  
6 system and  
7 wherein the processing system has a processing core that includes:  
8 a processing unit;

9                   an instruction cache for storing instructions for non-time-critical tasks and a  
10       code random access memory for storing instructions required for causing serving of time-  
11       critical tasks, the instruction cache and the code random access memory coupled to the  
12       processing unit;  
13                   a register group for updating status of registers related to time critical tasks;  
14       and  
15                   another register group coupled to the processing unit;  
16                   a data memory and another data memory coupled to the processing unit;  
17       and  
18                   wherein the processing unit need access status of registers only in the register  
19       group for execution of time-critical tasks thereby avoiding saving and restoring status of  
20       the another registers for execution of time-critical tasks.

1       Claim 42 (previously presented): The audio and video encoder/decoder according to  
2       Claim 41, wherein one of the time-critical tasks is providing additional data to a video  
3       engine unit during a video compression process.

1       Claim 43 (previously presented): The audio and video encoder/decoder according to  
2       Claim 42, wherein the additional data is provided to the video engine unit within a time  
3       interval of less than two microseconds.

1       Claim 44 (previously presented): The audio and video encoder/decoder according to  
2       Claim 41, wherein one of the non-time critical tasks is multiplexing of audio and video  
3       streams.

1       Claim 45 (previously presented): The audio and video encoder/decoder according to  
2       Claim 41, wherein one of the non-time-critical tasks is demultiplexing Motion Picture  
3       Expert Group (MPEG) streams.

1      Claim 46 (previously presented): The audio and video encoder/decoder according to  
2      Claim 41, wherein the non-time-critical tasks are user interface applications.

1      Claim 47 (previously presented): The audio and video encoder/decoder according to  
2      Claim 46, wherein one of the user interface applications is providing an on-screen display  
3      every two seconds.